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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
BROPHY, JAMIE LYNN

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/986,167	Applicant(s) LANE ET AL.	
	Examiner J. L. Brophy	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *22-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the election filed 6/6/03.

Election/Restrictions

Applicant's election with traverse of claims 1-21 in Paper No. 7 is acknowledged. The traversal is on the ground(s) that the examiner has not made a showing of separate classification, status, or field of search. This is not found persuasive because the claimed species are independent inventions and, therefore, it is not necessary to show a separate status in the art or separate classification (MPEP 808.01(a)). Applicant also traverses on the grounds that it would not be a serious burden for the examiner to examine the claims reading upon both species. Even though the second species includes only one non-generic claim, it would still be a burden on the examiner to examine two inventions at once. A reference that may be used to reject species I may not necessarily be used to reject species II and, therefore, it would be a burden on the examiner to search two independent inventions at once.

The requirement is still deemed proper and is therefore made FINAL.

Claim 22 is withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 7.

Claim Objections

Claims 1 and 17 are objected to because of the following informalities:

In claim 1, line 5, there is insufficient antecedent basis for the limitation "said substrate" and should be "a substrate".

In claim 17, the limitation of said first conductors being N-type is unclear since the first conductors are "first *metal* conductors" (see claim 7, line 10). It is unclear how a metal can be N-type.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 7-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moise et al (6,534,809) in view of Jeng et al (5,893,734).

Moise et al teach a method that comprises forming a pair of spaced word lines;

Forming source and drain regions on opposite sides of the word lines to define a plurality of memory cell access transistors 106 within a memory cell array area 103;

Forming a pair of access transistors 106 sharing a source/drain region 108;

Forming at least one first insulating layer 112 over the access transistors 106;

Forming a pair of capacitor polysilicon plugs 114 and a bit line polysilicon plug 114 through the first insulating layer 112 to the source and drain regions 108 of the access transistors 106;

Forming at least one second insulating layer 134 over the polysilicon plugs 114;

Forming container capacitors 125 respectfully associated with each of the access transistors 106 in the second insulating layer 134 over and in electrical communication with respective capacitor polysilicon plugs 114;

Heat treating the container capacitors 125 (col. 9, lines 45-52, col. 10, lines 16-26 and 59-61);

Forming N-channel or P-channel peripheral logic transistors in a peripheral circuitry area 105;

Forming peripheral metal plugs 136 through the second insulating layer 134 to contact the N-channel or P-channel peripheral logic transistor after the heat treating;

Forming at least one third insulating layer 160 over the container capacitors 125;

Forming a bit line contact 136 through the second insulating layer 134 to the bit line polysilicon plug 114 after the heat treating at the same time as the peripheral metal plugs are formed, wherein the bit line contact is formed of metal (col. 8, lines 29-33); and

Forming metal contacts 150 through the third insulating layer 160 to the peripheral metal plugs 136 and the bit line contact 136.

See Fig. 1 and accompanying text.

However, Moise et al do not specifically teach that the peripheral circuitry area includes an N-channel and a P-channel transistor and a metal plug contacting each of the transistors.

Jeng et al teach providing an N-channel and a P-channel transistor in the peripheral circuitry area (col. 5, lines 11-14).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Moise et al by forming both N-channel and P-channel transistors in the peripheral circuitry area because a person of ordinary skill in the art at the time the invention was made would have been motivated to provide both N-channel and a P-channel transistors in the peripheral circuitry area since it is well known in the art to have both N-channel and a P-channel transistors in the peripheral circuitry area (see Jeng et al, col. 5, lines 11-14). In addition, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Moise et al by providing metal plugs to contact the N-channel and P-channel transistors in the peripheral circuitry area because a person of ordinary skill in the art at the time the invention was made would have been motivated to provide metal plugs to contact the N-channel and P-channel transistors in the peripheral circuitry area in order to provide communication between the N-channel and P-channel transistors and subsequent devices (see Shukuri et al, Fig. 4).

Re claims 10 and 13-16, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select an appropriate size and shape of the metal plug layers. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or

in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from results of prior art...such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality...More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Claims 1-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (6,200,855) in view of Moise et al.

Lee teaches a method that comprises forming a pair of spaced word lines;

Forming source and drain regions on opposite sides of the word lines to define a plurality of memory cell access transistors 104 within a memory cell array area;

Forming a pair of access transistors 104 sharing a source/drain region;

Forming at least one first insulating layer 108 over the access transistors 104;

Forming a pair of capacitor polysilicon plugs 110b and a bit line polysilicon plug 110a through the first insulating layer 108 to the source and drain regions of the access transistors 104;

Forming at least one second insulating layer 126 over the polysilicon plugs 110a, 110b;

Forming container capacitors respectfully associated with each of the access transistors in the second insulating layer 126 over and in electrical communication with respective capacitor polysilicon plugs 110b;

Forming N-channel and P-channel peripheral logic transistors in a peripheral circuitry area;

Forming peripheral metal plugs 128a through the first 108 and second 126 insulating layer to contact the N-channel and P-channel peripheral logic transistors (col. 6, lines 53-58);

Forming at least one third insulating layer 131 over the container capacitors; and

Forming metal contacts 133 through the third insulating layer 131 to contact the peripheral metal plugs 128a.

See Figs. 2A-2D and accompanying text.

In addition, Lee teaches that excessive heat is released during the capacitor forming process. However, Lee does not specifically teach the step of heat treating the capacitor, wherein the heat treatment may be performed prior to forming the upper electrode or after all portions of the capacitors are formed.

Moise et al teach the step of heat treating a capacitor, wherein the heat treatment may be performed prior to forming the upper electrode or after all portions of the capacitors are formed (col. 10, lines 17-26).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Lee by performing a heat treatment on the capacitors because a person of ordinary skill in the art at the time the

invention was made would have been motivated to perform a heat treatment on the capacitors in order to crystallize the dielectric layer or control the stress in the electrodes (see Moise et al, col. 9, lines 45-52 and col. 10, lines 17-26 and 59-61).

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moise et al in view of Jeng et al and further in view of Tu et al (6,294,426).

Moise et al teach a method that comprises forming a pair of spaced word lines;

Forming source and drain regions on opposite sides of the word lines to define a plurality of memory cell access transistors 106 within a memory cell array area 103;

Forming a pair of access transistors 106 sharing a source/drain region 108;

Forming at least one first insulating layer 112 over the access transistors 106;

Forming a pair of capacitor polysilicon plugs 114 and a bit line polysilicon plug 114 through the first insulating layer 112 to the source and drain regions 108 of the access transistors 106;

Forming at least one second insulating layer 134 over the polysilicon plugs 114;

Forming container capacitors 125 respectfully associated with each of the access transistors 106 in the second insulating layer 134 over and in electrical communication with respective capacitor polysilicon plugs 114;

Heat treating the container capacitors 125 (col. 9, lines 45-52, col. 10, lines 16-26 and 59-61);

Forming N-channel or P-channel peripheral logic transistors in a peripheral circuitry area 105;

Forming peripheral metal plugs 136 through the second insulating layer 134 to contact the N-channel or P-channel peripheral logic transistor after the heat treating;

Forming at least one third insulating layer 160 over the container capacitors 125;

Forming a bit line contact 136 through the second insulating layer 134 to the bit line polysilicon plug 114 after the heat treating at the same time as the peripheral metal plugs are formed, wherein the bit line contact is formed of metal (col. 8, lines 29-33); and

Forming metal contacts 150 through the third insulating layer 160 to the peripheral metal plugs 136 and the bit line contact 136.

See Fig. 1 and accompanying text.

However, Moise et al do not specifically teach that the peripheral circuitry area includes an N-channel and a P-channel transistor and a metal plug contacting each of the transistors. In addition, Moise et al do not teach that the method for forming the capacitors comprises etching through the second insulating layer and portions of the capacitor plugs to form capacitor container openings; depositing a conductive layer with the capacitor container openings to form a bottom layer; planarizing an upper surface of the capacitor containers to remove any conductive layer material on the upper surface; depositing a dielectric layer over the substrate; and depositing an upper capacitor plate over the dielectric layer.

Jeng et al teach providing an N-channel and a P-channel transistor in the peripheral circuitry area (col. 5, lines 11-14).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Moise et al by forming both N-channel and P-channel transistors in the peripheral circuitry area because a person of ordinary skill in the art at the time the invention was made would have been motivated to provide both N-channel and a P-channel transistors in the peripheral circuitry area since it is well known in the art to have both N-channel and a P-channel transistors in the peripheral circuitry area (see Jeng et al, col. 5, lines 11-14). In addition, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Moise et al by providing metal plugs to contact the N-channel and P-channel transistors in the peripheral circuitry area because a person of ordinary skill in the art at the time the invention was made would have been motivated to provide metal plugs to contact the N-channel and P-channel transistors in the peripheral circuitry area in order to provide communication between the N-channel and P-channel transistors and subsequent devices (see Shukuri et al, Fig. 4).

Tu et al teach a method for forming a capacitor that comprises etching through the second insulating layer 16 and portions of the capacitor plugs 14a to form capacitor container openings 19; depositing a conductive layer with the capacitor container openings 19 to form a bottom layer 20; planarizing an upper surface of the capacitor containers 19 to remove any conductive layer material on the upper surface; depositing a dielectric layer 21 over the substrate; and depositing an upper capacitor plate 22a over the dielectric layer 21. See Figs. 7-13 and accompanying text.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Moise et al in view of Jeng et al by forming the capacitors using the method taught by Tu et al because a person of ordinary skill in the art at the time the invention was made would have been motivated to use the capacitor-forming method taught by Tu et al in order to increase the capacitance of the capacitor due to increased vertical dimensions (see Tu et al, col. 1, lines 51-59).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. L. Brophy whose telephone number is (703) 308-6182. The examiner can normally be reached on M-F (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

J.L.B.

jlb
June 15, 2003

AMIR ZARABIAN
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